



**Press release**

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## **Vector Fabrics joins forces with consortium led by Thales to ease parallel software development and increase battery life**

**Eindhoven, The Netherlands, January 31<sup>st</sup>, 2012** -- Vector Fabrics today announced it is joining forces with Thales to alleviate the issues involved in developing software for today's increasingly parallel architectures, while reducing power consumption. Over the last few years, electronic devices have greatly expanded their functionality. Rich graphical user interfaces, high-speed internet access, high-quality photo and video cameras and 3D gaming are all integrated into one device that easily fits in the palm of your hands. However, the underlying parallel hardware architectures that enable this functionality have introduced two new complications that will be addressed in this joint effort: programming complexity and power consumption.

Mike Beunder, CEO of Vector Fabrics says: "Writing multicore and parallel software is extremely difficult, bordering on the impossible. We often say you need to be a ninja or black belt programmer to complete such a mission. We're excited to be working together with these industry and academic leaders to further enhance our development tools that allow every software developer to become such a ninja programmer."

Prof. Albert Cohen from INRIA and École Normale Supérieure says: "Embedded system designers are getting increasingly involved in target-specific adaptation for complex multiprocessor systems-on-chip (MPSoC). To preserve functional correctness of the applications from these manual optimizations, the PHARAON project (Parallel and Heterogeneous Architectures for Real-time ApplicatiONs),

supported by the European Commission, advocates for sound concurrency and software engineering practices, driven by a new generation of analysis and code generation tools.”

Working together as a team, Vector Fabrics and Thales’ objective is to assist the designer in finding the most adequate software architecture taking into account hardware constraints. Accompanying the effort are Politecnico di Torino (Italy), École Normale Supérieure and INRIA (France), Interuniversitair Micro-Electronica Centrum (Belgium), University of Cantabria (Spain) and Tedesys (Spain). The group’s tools will be capable of evaluating the parallel structure of an application and propose improvements, handle communications between different processors and generate the multi-processor embedded code. In addition, a set of techniques and tools will impact the runtime behaviour of the application. The objective is to adapt the performance of the platform, for example by adjusting the frequency and voltage, in order to consume only the required energy to perform a specific task.

In order to warrant the real-world applicability of these newly-developed tools and software, the three-year project will develop proof-of-concept demonstrations in two application domains: lower-power, higher-quality digital radio communications and image vision for automotive applications, such as stereoscopic camera-based obstacle detection and collision avoidance. The overall target is to reduce software development cost by 25% and decrease the power consumption of embedded systems by nearly 20%.

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